

Intel's Investigation of Next-Generation Memory Technologies for Portable Devices

Stefan Lai

Vice President, TMG, Intel Corporation

Co-Director, California Technology and Manufacturing

July 2001

Agenda

- **Intel's Research Model**
- **Need for Next-Generation Memories**
- **Polymer Memories for Data Storage**
- **Ovonics Unified Memory (OUM) for Code + Data Storage**

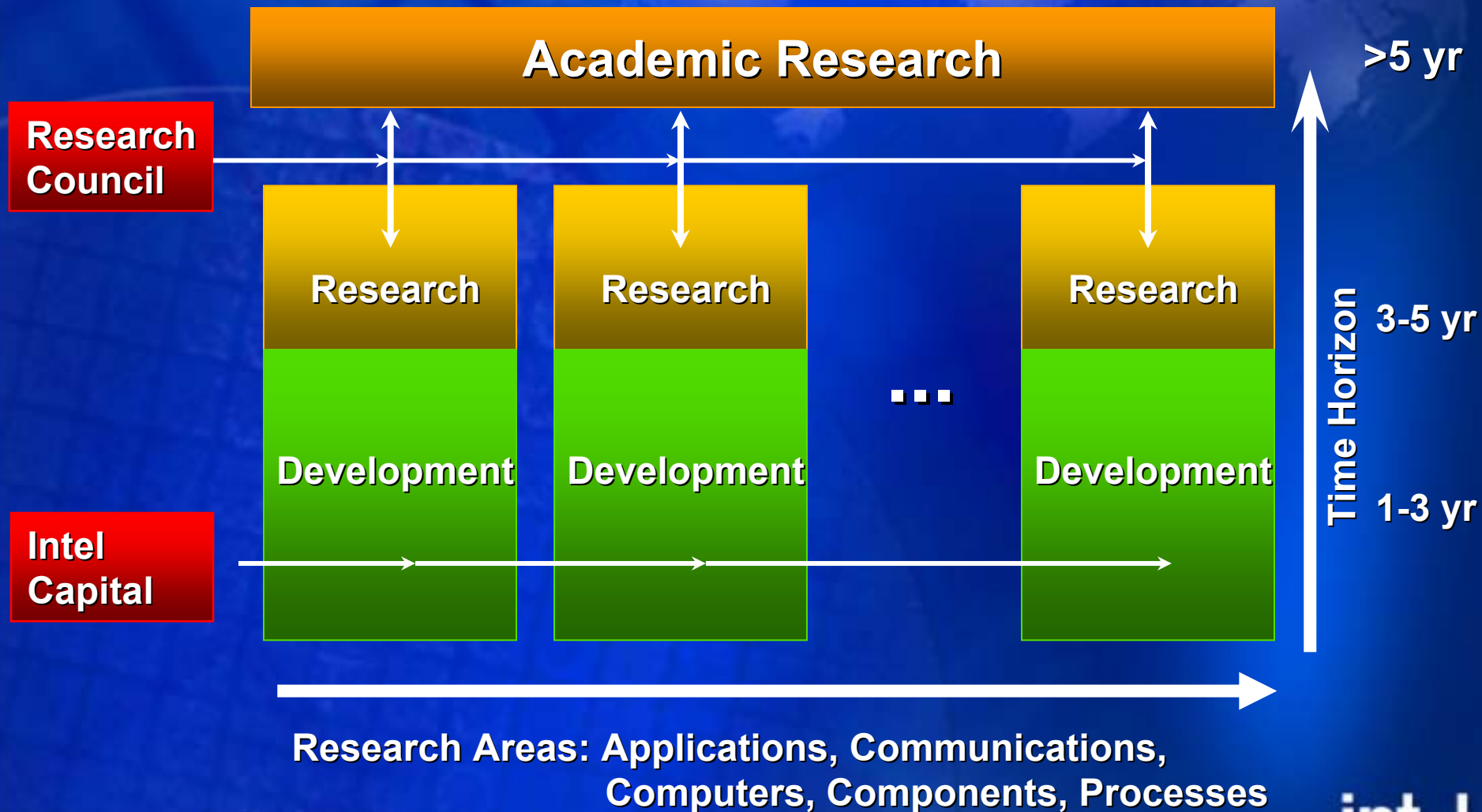
Intel's Research Model

- Internal research focus
- External research sponsorship
- Technology transfer

Internal Research: Intel's Research Labs

- **3 primary research labs**
 - Intel Architecture Labs
 - Microcomputer Research Labs
 - Components Research
- **> 750 researchers internationally**

Long-Term Research and Near-Term Development



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- Ovonics Unified Memory (OUM) for code+data storage

Need for Next-Gen Memories

- Industry searching for “Holy Grail” future memory technologies for portable devices (cell phones, mobile PCs, etc.)
 - Desired memory attributes: Low cost, low power, non-volatile and easy to integrate
- Today’s memory technologies each have limitation(s)
 - DRAM is volatile and difficult to integrate
 - SRAM is high cost and volatile
 - Flash has slower writes and limited number of write/erase cycles compared to others
- Several next-generation memory technologies are being studied, including MRAM, FeRAM, Polymer Memory and Ovonic Unified Memory (OUM)

New Memories To Improve Performance of Wireless Devices



Home



**Web
Tablet**



**Two-Way
Pagers**



Phones



PIDs



Business



Hybrid Devices



**In-Car Computing
Telematics**



On The Move



**Wearable
Computing**

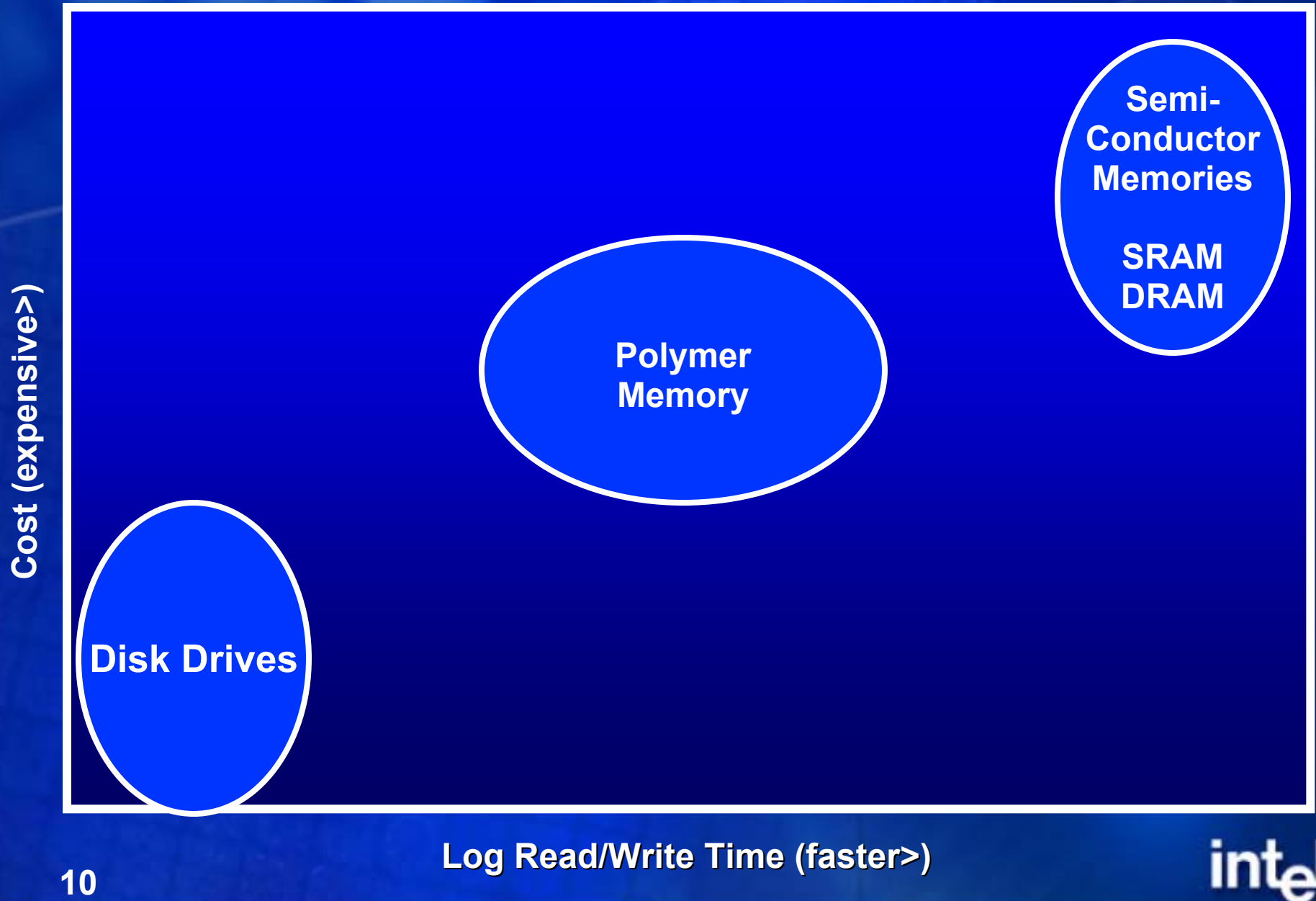


micronotebook

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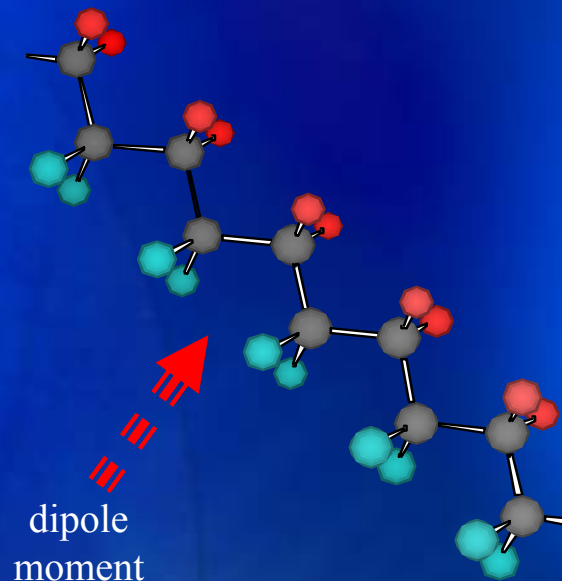
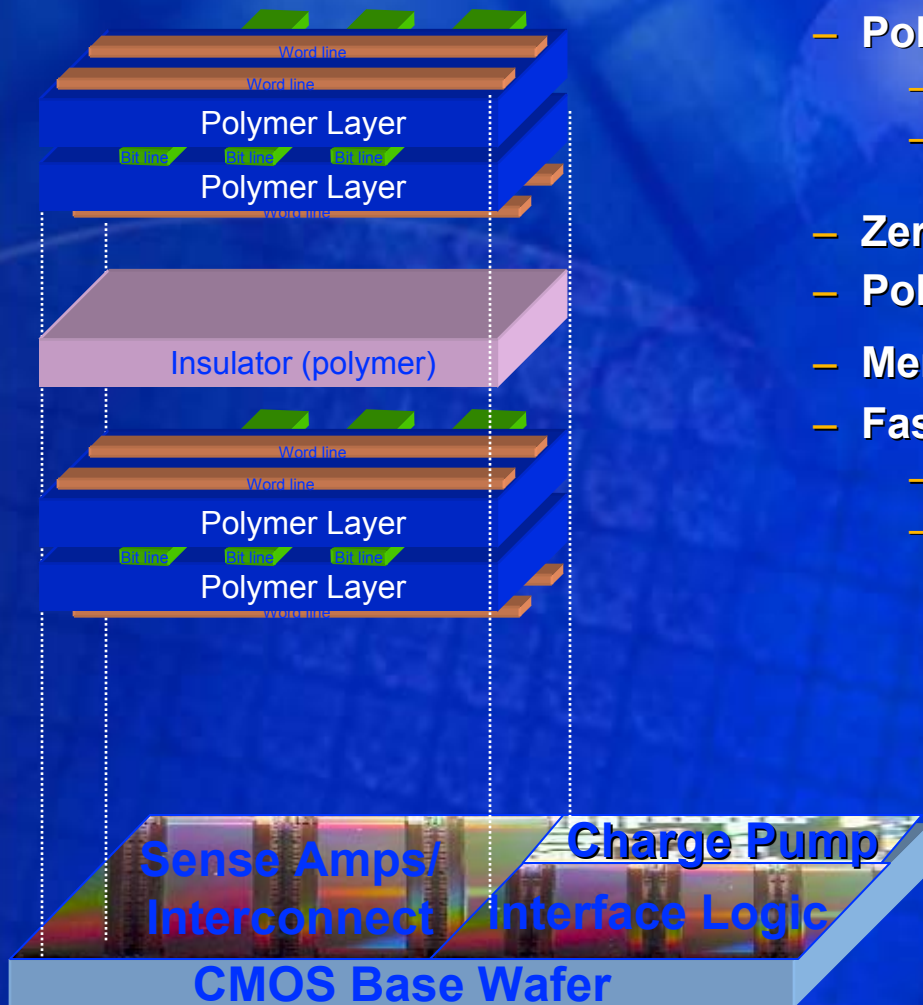
Memory Technologies Comparison



What Is Polymer Memory?

- Attributes

- Polymeric Ferroelectric RAM (PFRAM)
 - Polymer chains with a dipole moment
 - Data stored by changing the polarization of the polymer between metal lines
- Zero transistors per bit of storage
- Polymer layers can be stacked
- Memory is NON-Volatile
- Fast read and write speeds
 - Microsecond initial reads
 - Write speed faster than NAND and NOR Flash



What Is Polymer Memory? (cont.)

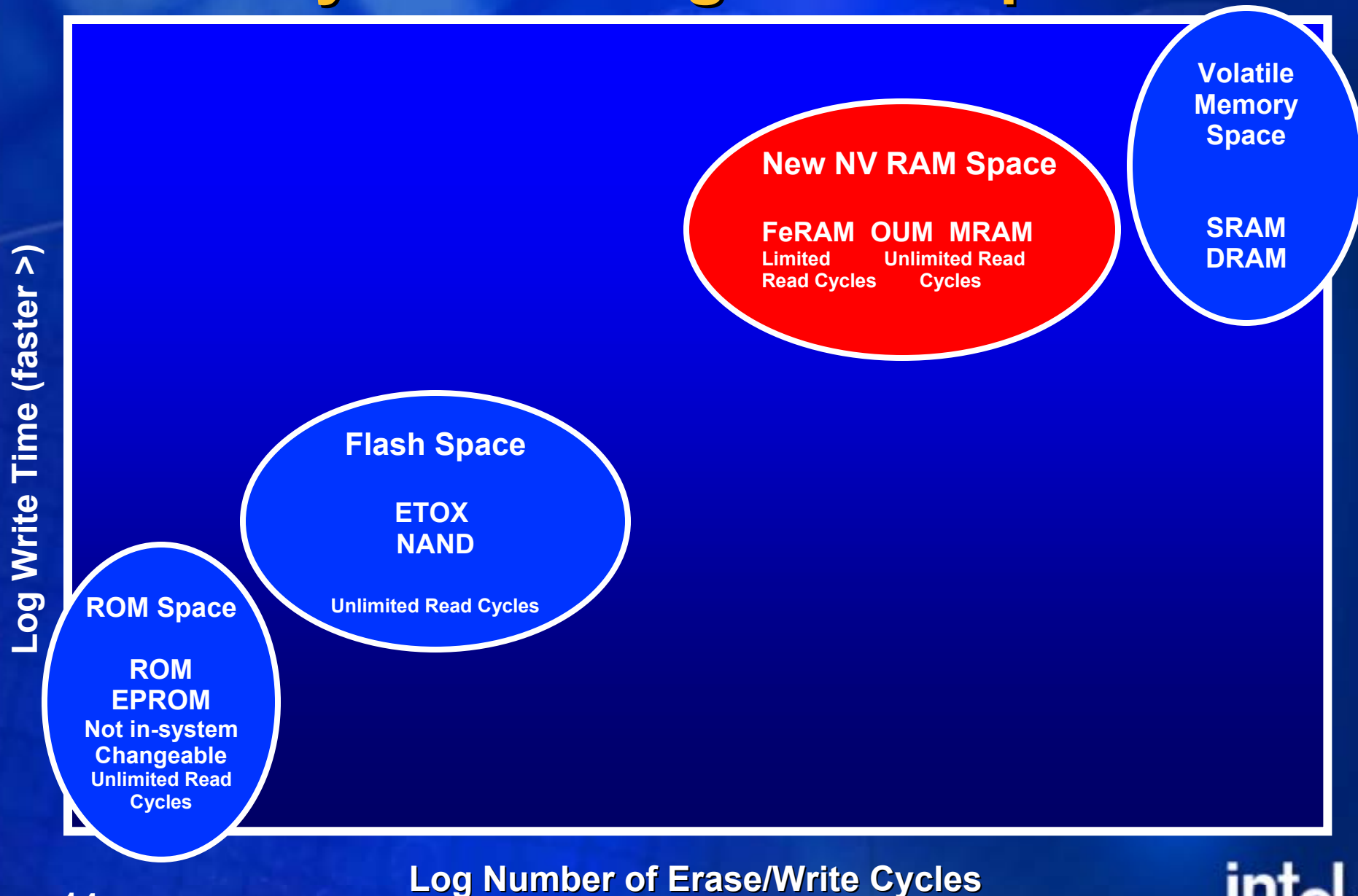
● Attributes

- Very low cost/bit, high capacity per dollar
 - Simple processing, easy to integrate with other CMOS
 - $4\lambda^2$ cell size is effectively $\frac{1}{2}\lambda^2$ with 8 layers stacked (vs. $3\lambda^2$ for 2 bit/cell NAND)
- Low power consumption
 - No cell standby power or refresh required
- Test memory arrays have been fabricated in joint development with Thin Film Electronics ASA
 - TFE is an Intel Capital portfolio company with technology development operations based in Linköping, Sweden
 - Joint technology development ongoing
 - Intel has an option to license TFE's technology
- PFRAM low-cost/high capacity fits well in handheld data storage applications

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Memory Technologies Comparison



Next-Generation Code + Data Memory Technology Camps

MRAM

IBM

Motorola

Infineon

OUM

Ovonyx

Intel

ST Micro

British Aerospace

FRAM

Ramtron

Fujitsu

Toshiba

Samsung

Hitachi

IBM / Infineon

Symetrix

Matsuhita

Motorola

Micron

NEC

** Other brands and names are the property of their respective owners*

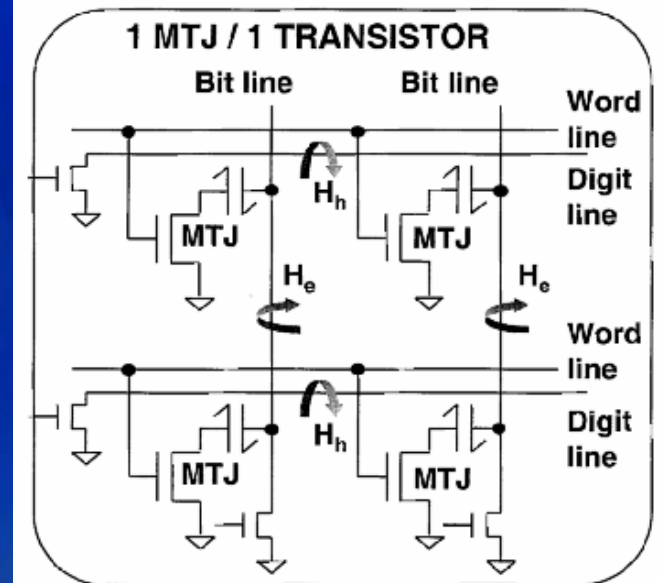
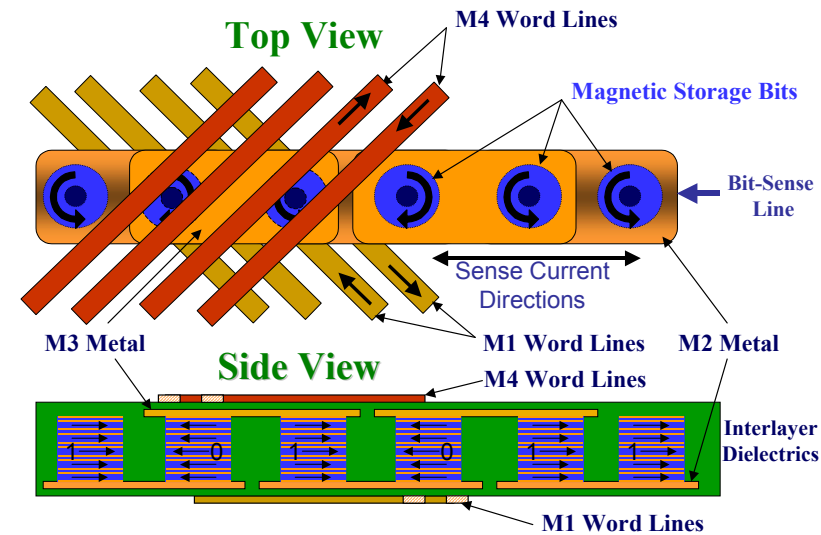
What Is MRAM?

- **Operation**

- Cell is 1 MJT + 1 Transistor
- Electric current switches the magnetic polarity
- Change in magnetic polarity sensed as resistance change

- **Attributes**

- + Non-Volatile
- + High Density
- + Non Destructive Read
- + Low Voltage & Low Power
- + Write = Read Speed, < 50 nsec
- + Unlimited R/W Endurance
- Material compatibility with CMOS a key challenge



What Is FeRAM?

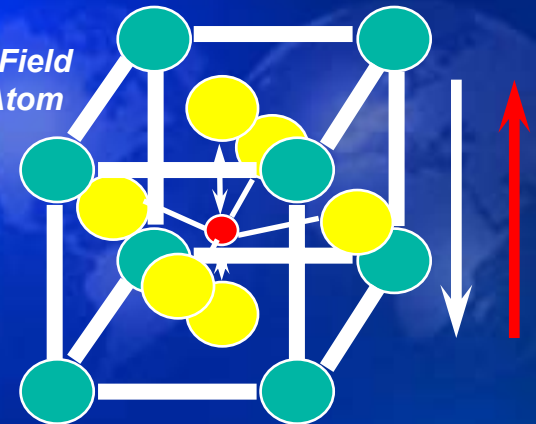
● Operation

- Selected crystalline materials have bi-stable center atom
- Data is stored by applying an voltage to polarize the internal dipoles “Up” or “Down”
- Non-Linear FRAM Read Capacitor
- No iron, no magnetism

● Attributes

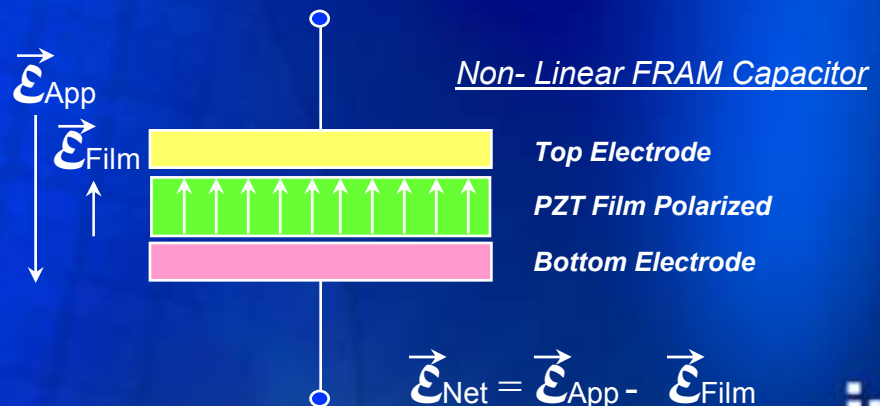
- + Non-Volatile
- + “Fast” Random Read Access
- + Fast Write with very low power consumption
- Destructive read, limited read and write cycles

Applied Electric Field
Moves Center Atom



Perovskite Crystal Unit Cell
PZT ($\text{PbO}, \text{ZrO}_2, \text{TiO}_2$) Lead-Zirconate-Titanate

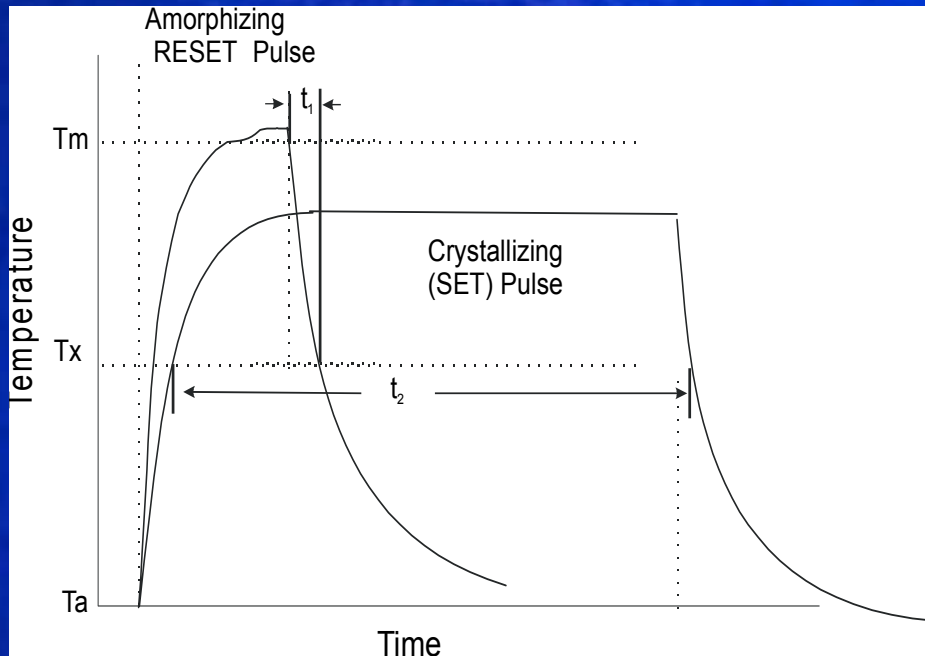
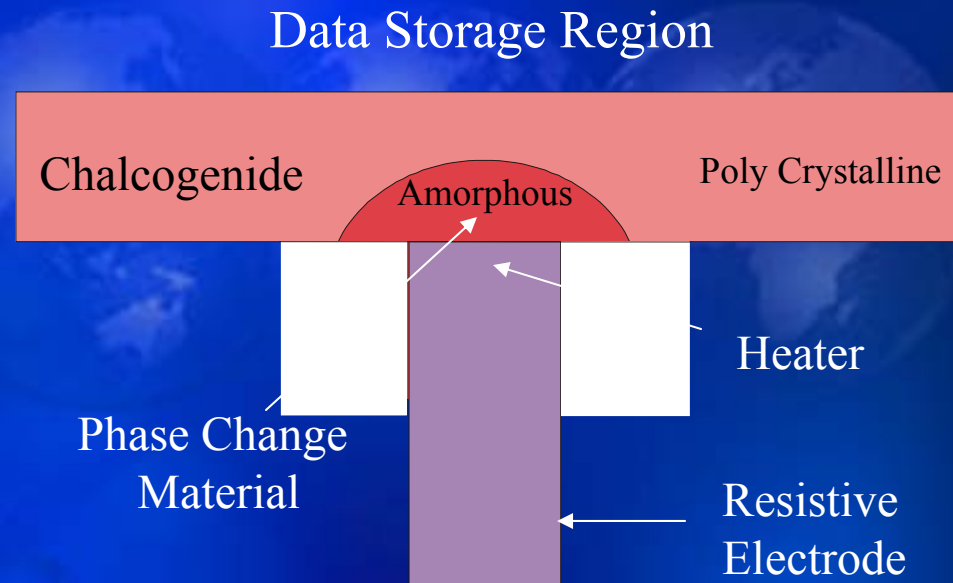
- Tetra/Pentavalent Atom
- Di/Monovalent Metal Atoms
- Oxygen Atoms



What Is OUM?

• Operation

- Chalcogenide material alloys used in re-writable CDs and DVDs
- Electrical energy (heat) converts the material between crystalline (conductive) and amorphous (resistive) phases
- Cell reads by measuring resistance



• Attributes

- + Non-volatile
- + High density
- + Non-destructive read
- + Low voltage and low power
- + $\sim 10^{12}$ write/erase cycles
- + Easy to integrate w/ logic

OUM in 1970

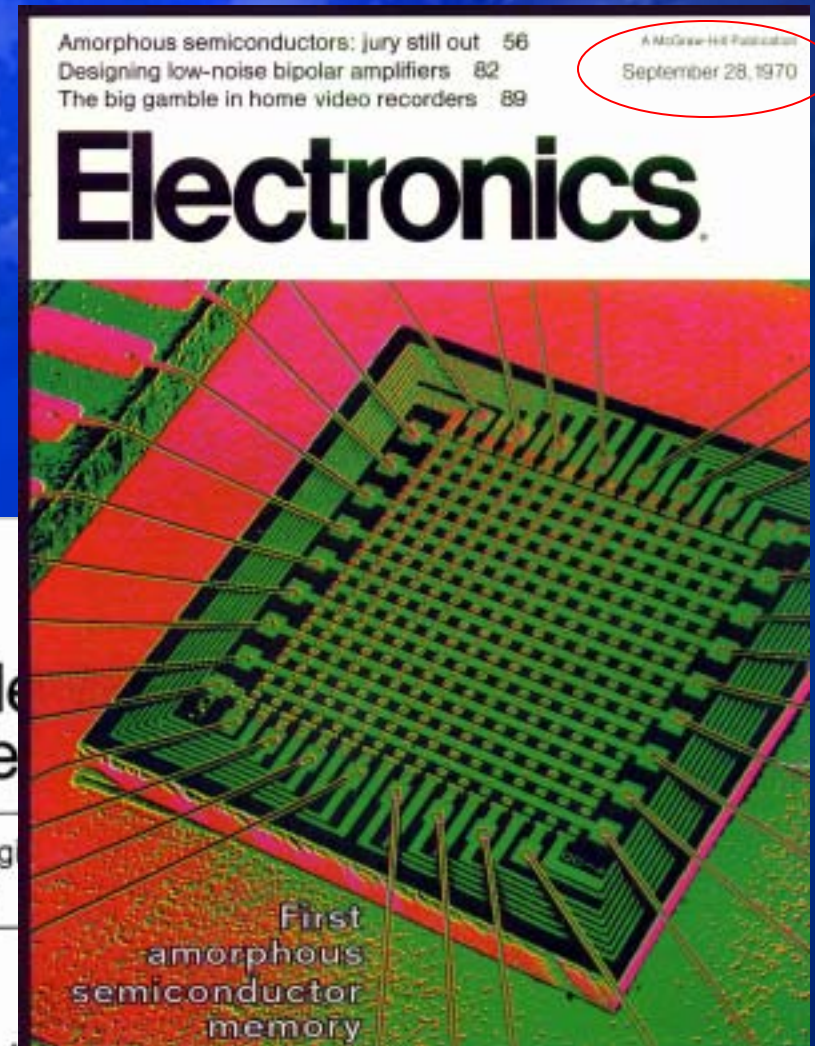
- Chalcogenide memories have been studied for > 30 years

Amorphous semiconductors Part I

Nonvolatile and reprogrammable the read-mostly memory is here

Integrated arrays combine amorphous and crystalline technology
new memories could help realize promise of microprogramming

By R. G. Neale and D. L. Nelson, Energy Conversion Devices Inc., Troy, Mich.
Gordon E. Moore, Intel Corp., Mountain View, Calif.



Why OUM Now?

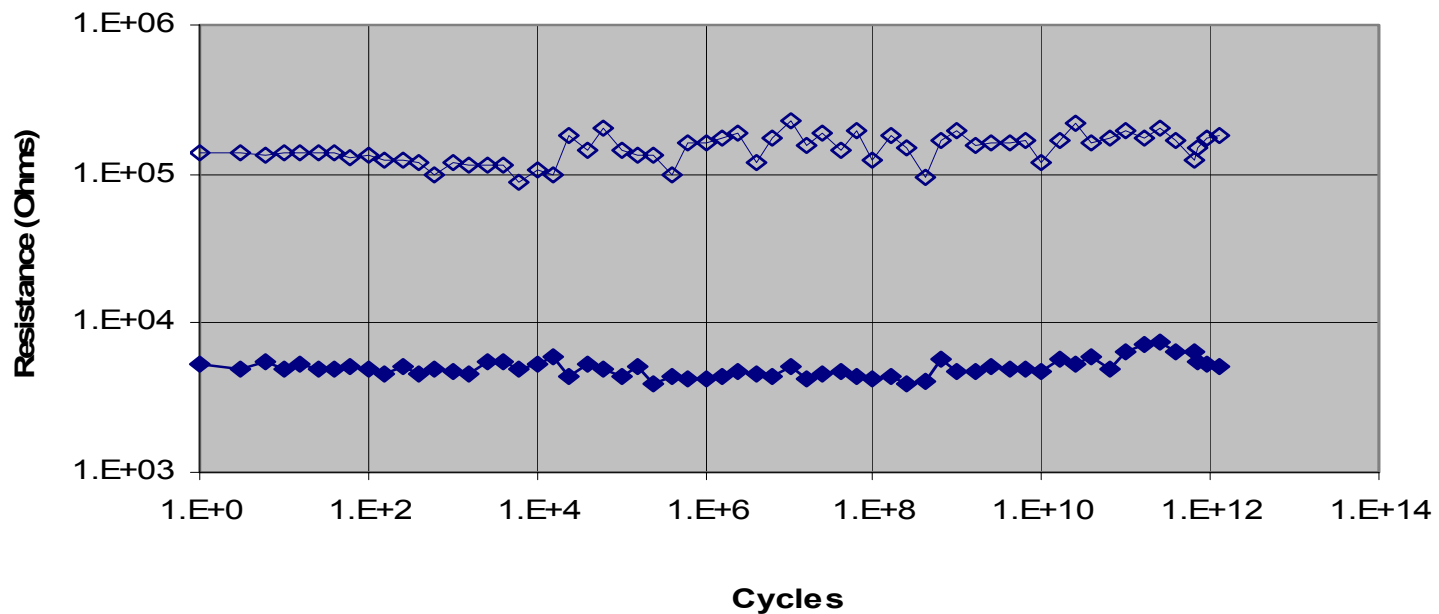
- **Material technologies have benefited from 30 years of silicon manufacturing learning**
 - High purity, thin film material can be prepared routinely
- **Significant chalcogenide material improvement has lead to successful CD-RW and DVD-RW products**
- **New cell physics understanding leading to new cell structure design**

OUM Test Chip

- OUM single cell works, challenge is in making high density arrays
- 4M test chips based on 180 nm lithography have been fabricated
- Test chip is functional, demonstrating basic cell and array operation in small dimensions
- Test chip is a good vehicle for further detail of cell optimization as well as manufacturability and reliability study

OUM Cycling Characteristics

OUM Endurance Cycling



—◆— Rset

—◆— Rreset

OUM As A Disruptive Memory Technology for Code + Data

- OUM is NOT a perfect memory
- <100 nSec write performance is “good enough” for many portable devices limited by wireless bandwidth and battery power
- OUM cycling is “good enough” for most code and data storage application
- One memory for most applications, only small amount of DRAM/SRAM needed for cache and other frequent write functions

OUM Compared to Other Code + Data Memories

- MRAM higher write and cycling performance, but more expensive
- FeRAM limited in cycling, also more expensive
- OUM has good write and cycling performance, smaller cell and easier to integrate: Best tradeoff for low cost portable devices

Next Steps for OUM Program

- Program in R&D stage, challenge to introduce new material in silicon process
- Test chip will allow process improvement and extensive data collection on manufacturability and reliability
- Not ready for product plan and schedule

Summary

- Many candidates for next generation non-volatile memory technologies->new market and business opportunity
- Intel is working on a number of options, including polymer memories for low cost data storage and OUM for code + data memories